# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/515,376 | 02/29/2000 | Sandeep Bhutani | 30454-00243(LSI C4-4247) | 1883 |

| 24319        7590        01/14/2004 | EXAMINER |
|---|---|
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| MS: D-106 LEGAL | ART UNIT | PAPER NUMBER |
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| MILPITAS, CA  95035 | 2128 | |

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ___3___ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *Oct. 22, 2003* _____.

2a) ☐ This action is **FINAL**.      2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1-22* _____ is/are pending in the application.

     4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-22* _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

     If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a) ☐ All b) ☐ Some* c) ☐ None of:

         1. ☐ Certified copies of the priority documents have been received.

         2. ☐ Certified copies of the priority documents have been received in Application No. _____.

         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     *See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

     a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)      4) ☐ Interview Summary (PTO-413) Paper No(s). _____

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)      5) ☐ Notice of Informal Patent Application (PTO-152)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____      6) ☐ Other:

## DETAILED ACTION

This Office Action is in response to applicants' amendment filed on Oct. 22, 2003.

Claims 1-22 are pending in this Office Action.

### *Drawings*

1.    This application has been filed with informal drawings which are acceptable for

examination purposes only.  Formal drawings will be required when the application is allowed.

### *Double Patenting*

2.    The nonstatutory double patenting rejection is based on a judicially created doctrine

grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees.  See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619

(CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to

overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this

application.  See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

3.    Claims 1-22 are rejected under the judicially created doctrine of obviousness-type double

patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,484,297. Although the

conflicting claims are not identical, they are not patentably distinct from each other because the

present claimed invention and claims in the US patent are directed to a method and system for

characterizing delays of a cell in an integrated circuits under various operating conditions. The

delay characterization is modeled based on cell operation parameters and parameter values for

various operation conditions such as normal operation, worst condition, etc. The delay

characterization processes are obvious and presented in a manner that the parameter factors

would include conditions for normal operations as claimed herein.

*Claim Rejections - 35 USC § 103*

4.    The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth
> in section 102 of this title, if the differences between the subject matter sought to be patented and the prior
> art are such that the subject matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be
> negatived by the manner in which the invention was made.

5.    Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rigg et al.,

US patent no. 5,802,349.

As per claim 1, Rigg discloses a method and system for computing delays of a cell in an

integrated circuit with feature limitations substantially similar to the claimed invention.

According to Rigg, the method includes steps:

generating a first set of the delays of the cell by assigning values to the cell parameters

(col. 3, lines 4-17) including nominal values for circuit operations for normal circuit operation,

generating a second set of the delays of the cell by varying values assigned to the

parameters of the cell (col. 3, lines 18-57),

creating a delay equation based on the first and second set of cell parameters (cols. 4-6),

and calculating cell delay using the delay equation, wherein the delay equation

characterizes the delays in terms of the cell parameters (cols. 4-6). Rigg does not expressly

disclose assigning nominal values to the cell parameter in the cell characterization process as

claimed.

Practitioner in the art at the time of the invention was made would have found Rigg

disclosure of cell operation characterization above with the features of cell operating parameters

for circuit cells operations obviously includes assigning nominal values for cell parameters for

normal operation and/or best/worst operation conditions in common cell design practices.

As per claim 2, Rigg discloses cell operation (cols. 3-4) would obviously imply the

limitations of setting cell parameters to nominal values.

As per claim 3, Rigg discloses varying rise/fall edge rate ratio or input ramptime in

deriving delay factor for cell characterization (cols. 5, 6).

As per claim 4, Rigg discloses best/worst rise/fall edge rate or ramptime which could include a minimum input ramptime and a maximum allowable ramptime.

As per claim 5, Rigg disclosure would include best/worst load capacitance including a minimum allowable and maximum allowable capacitance load as claimed.

As per claim 6, Rigg discloses varying process to a non-nominal process for worst and best analysis.

As per claims 7 and 8, Rigg discloses non nominal circuit operation which implies varying temperature and supply voltage to non nominal values to analyze worst and best case conditions (cols. 3-5).

As per claims 9-10, Rigg discloses varying ramptime and load capacitance as claimed (cols. 4-5).

As per claim 11-12, Rigg discloses delay characterization are computationally generated as function of circuit operation parameters such as power supply, operating temperature, process variation, capacitance load, etc.

As per claim 13, Rigg discloses a method and system for computing delays of a cell in an integrated circuit with feature limitations substantially similar to the claimed invention. According to Rigg, the method includes steps of

generating a first set of the delays of the cell by assigning values to the cell parameters (col. 3, lines 4-17) including nominal values for normal cell operation,

generating a second set of the delays of the cell by varying values assigned to the parameters of the cell (col. 3, lines 18-57),

creating a delay equation based on the first and second set of cell parameters (cols. 4-6),

and calculating cell delay using the delay equation, wherein the delay equation

characterizes the delays in terms of the cell parameters (cols. 4-6). Rigg does not expressly

disclose assigning nominal values to the cell parameter in the processes of cell characterization

as claimed.

Practitioner in the art at the time of the invention was made would have found Rigg

disclosure of cell operation characterization above with the features of cell operating parameters

for circuit cells operations obviously includes assigning nominal values for cell parameters for

normal circuit operation and/or best/worst operation conditions in cell design practices.

As per claim 14, Rigg discloses assigning parameter values for cell delay

characterization, which would include time value within the first range to the input ramptime of

the cell (cols. 5, 6), and load value within the second range (cols. 4-6).

As per claims 15-16, Rigg discloses generating delay equation with coefficients which is

function of circuit operation parameters such as process variation, nominal operating

temperature, power supply, capacitive load, ramptime, etc, and inserting such generated

coefficients into the delay equations for cell delay analysis.

As per claims 17 and 18, claims 17 and 18 are directed to the same apparatus in order to

perform steps of generating delay equation in a circuit cell as above. Rigg discloses a method

and system for computing delays of a cell in an integrated circuit with feature limitations

substantially similar to the claimed invention. According to Rigg, the method includes steps:

generating a first set of the delays of the cell by assigning nominal values to the cell

parameters (col. 3, lines 4-17) including,

generating a second set of the delays of the cell by varying values assigned to the

parameters of the cell (col. 3, lines 18-57),

creating a delay equation based on the first and second set of cell parameters (cols. 4-6),

and calculating cell delay using the delay equation, wherein the delay equation

characterizes the delays in terms of the cell parameters (cols. 4-6). Rigg does not expressly

disclose assigning nominal values to the cell parameter in the processes of cell characterization

as claimed.

Practitioner in the art at the time of the invention was made would have found Rigg

disclosure of cell operation characterization above with the features of cell operating parameters

for circuit cells operations obviously including cell normal operation and/or best/worst operation

conditions in cell design practices.

As per claim 19, claim 19 is directed to the same apparatus in order to perform steps of

generating delay equation in a circuit cell. Rigg discloses a method and system for computing

delays of a cell in an integrated circuit with feature limitations substantially similar to the

claimed invention. According to Rigg, the method includes steps:

generating a first set of the delays of the cell by assigning values to the cell parameters

(col. 3, lines 4-17) including nominal values assigned to cell parameters for normal circuit

operations,

generating a second set of the delays of the cell by varying values assigned to the

parameters of the cell (col. 3, lines 18-57),

creating a delay equation based on the first and second set of cell parameters (cols. 4-6),

and calculating cell delay using the delay equation, wherein the delay equation

characterizes the delays in terms of the cell parameters (cols. 4-6). Rigg does not expressly

disclose assigning nominal values to the cell parameter in the processes of cell characterization

as claimed.

Practitioner in the art at the time of the invention was made would have found Rigg

disclosure of cell operation characterization above with the features of cell operating parameters

for circuit cells operations obviously includes assigning nominal values for cell parameters for

normal operation and/or best/worst operation conditions in common cell design practices.

As per claim 20, Rigg discloses assigning time value within the first range to the input

ramptime of the cell (cols. 3-5), and load value within the second range.

As per claims 21-22, Rigg discloses generating delay equation with coefficients which is

function of circuit operation parameters such as process variation, nominal operating

temperature, power supply, capacitive load, ramptime, etc. and inserting such

## *Response to Arguments*

6.      Applicant's arguments with respect to claims 1-22 have been considered but are moot in

view of the new ground(s) of rejection.


## *Conclusion*

7.      Any inquiry concerning this communication or earlier communications from the examiner

should be directed to patent examiner Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703)305-3900.

**Any response to this action should be mailed to:**

Commissioner of Patents

P.O. Box 1450

Alexandria, VA 22313-1450


**or faxed to:**

(703) 872-9306, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal

Drive, Arlington. VA., Sixth Floor (Receptionist).

January 8, 2004

*thauphan*
*Patent Examiner*
Thai Phan
AU : 2128